APPLICATION NOTE

TDA9962 CCD
SIGNAL PROCESSOR

AN 02104

Philips
Semiconductors

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APPLICATION NOTE

TDA9962 CCD SIGNAL PROCESSOR

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Note: Due to the numerous similarities of the TDA9962 with the TDA9952, all the explanations and advices given in the TDA9952 application note AN01051 are also valid for the TDA9962, except for the PGA gain and the initial conditions of the serial interface which are explained in this document.

1 INTRODUCTION

The TDA9962 is an analog to digital interface for CCD based cameras. This chip includes a correlated double sampling block (CDS), an optical black calibration loop, a programmable gain amplifier (PGA), a low power 12-bits analog to digital converter (ADC) and an 8-bits digital to analog converter (DAC) for additional system controls. The PGA, DAC, black reference and other control pulses polarities are programmed through a simple 3 wires serial interface.

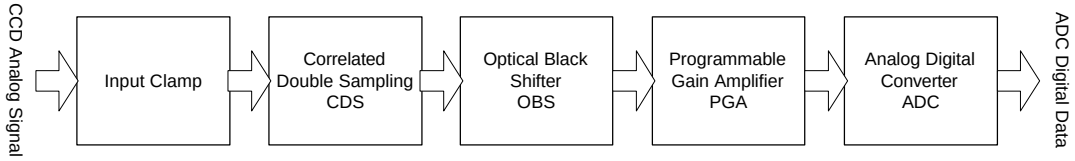

Figure 1. Philips CCD preprocessor features

2 PROGRAMMABLE GAIN AMPLIFIER

The goal of PGA is to amplify the differential voltage obtained thanks to the CDS to use the maximum input range of the ADC. The PGA gain is programmable from -2.5 dB to 21.5 dB via the 3 wires serial interface. Taking into account the gain of the other blocks, full scale output (code 0 to 4095 at ADC output) will be reached with an input amplitude ΔV_{DATA} of 800mV and the gain code setting 0.

The equation of gain, described on Figure 3, is the following:

$$Gain_{dB} = \left(\frac{Code}{255} * 24dB \right) - 2.5dB$$

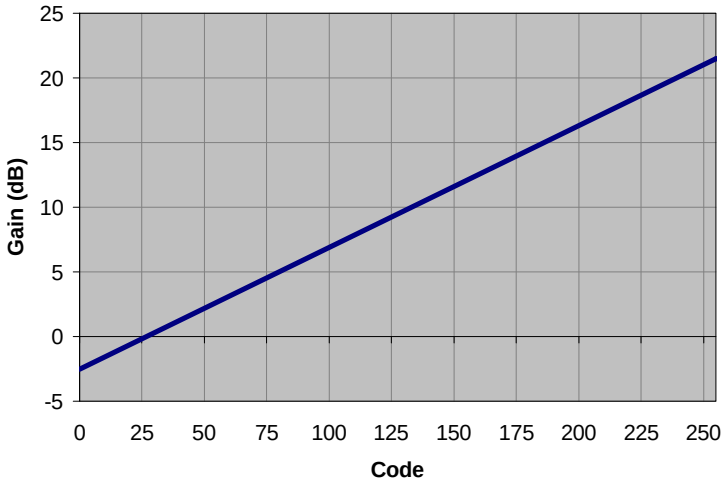

Figure 2. PGA Gain = f(Code)

The main characteristics of PGA are:

- Setting over 8 bits
- Gain range = 24dB
- Steps = 0.1dB +/- 0.02 dB
- Integral Non Linearity(max) = +/- 0.033dB

When the maximum ΔV_{DATA} value in mV (DataMax) on a frame is known, the code to be set in order to have a full scale output is given by the following equation:

$$Code = \frac{20 \cdot \log\left(\frac{800mV}{DataMax} \right)}{24dB} \cdot 255$$

It is also possible to set the PGA gain of TDA9962 from -2.5 dB to 33.5 dB in a continuous way. In order to activate this function, first it is necessary to send the following setting sequence in register of the serial interface:

Address bits A3 to A0					Data bits SD11 to SD0												Comment
3	2	1	0		11	10	9	8	7	6	5	4	3	2	1	0	
0	1	0	0		X	X	X	X	1	1	1	1	1	1	1	1	36 dB Gain Range

Then the equation of gain, described on Figure 3, is the following:

- For code between 0 and 383 : $Gain_{dB} = \left(\frac{Code}{383} * 36dB \right) - 2.5dB$
- For code between 383 and 511, gain is set to 33.5dB

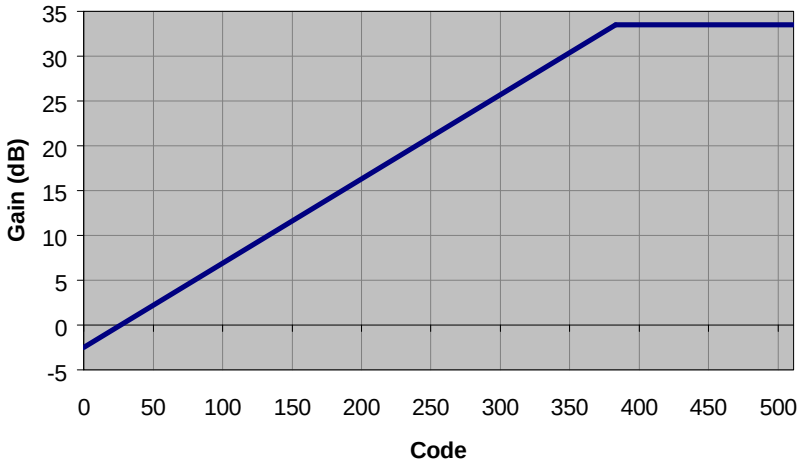

Figure 3. PGA Gain = f(Code)

The main characteristics of PGA are:

- Setting over 9 bits
- Gain range = 36dB
- Steps = 0.1dB +/- 0.02 dB
- Integral Non Linearity(max) = +/- 0.033dB

When the maximum ΔV_{DATA} value in mV (DataMax) on a frame is known, the code to be set in order to have a full scale output is given by the following equation:

$$Code = \frac{20 \cdot \log\left(\frac{800mV}{DataMax} \right)}{36dB} \cdot 383$$

3 CONTROL INPUTS

When power supplies increase from zero, the settings programmed by defect are:

- Polarity settings:

Address bits A3 to A0					Data bits SD11 to SD0												Comment
3	2	1	0		11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	1		X	X	0	1	1	1	1	1	1	1	1	1	All the control pulses are active on rising edge or high level.

- PGA gain code is set to 000
- Clamp code is set to 64
- Input OFD is set to logic 0